REMARKS

This application has been carefully reviewed in light of the Office Action dated October 5, 2006. Applicant has amended claim 1. Reconsideration and favorable action in this case are respectfully requested.

The Examiner has rejected claims 1 and 8 under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1 and 8 of U.S. Pat. No. 7,120,715. Applicants have reviewed this patent and disagree with the contention.

The Examiner has rejected claims 1-5, and 7 under 35 U.S.C. §103(a) as being unpatentable over U.S. Pat. No. 5,906,000 to Abe in view of U.S. Pat. No. 6,006,303 to Barnaby. Applicant has reviewed these references in detail and does not believe that they disclose or make obvious the invention as claimed.

The Examiner has rejected claims 8, 9 and 11 under 35 U.S.C. §103(a) as being unpatentable over U.S. Pat. No. 4,814,974 to Narayanan in view of U.S. Pat. No. 4,818,932 to Odenheimer and U.S. Pat. No. 5,581,722 to Welland. Applicant has reviewed these references in detail and does not believe that they disclose or make obvious the invention as claimed.

The Examiner has rejected claim 10 under 35 U.S.C. §103(a) as being unpatentable over U.S. Pat. No. 4,814,974 to Narayanan in view of U.S. Pat. No. 4,818,932 to Odenheimer and U.S. Pat. No. 5,581,722 to Welland and further in view of David Eck (xLogic CircuitsLab 2: Memory Circuits). Applicant has reviewed these references in detail and does not believe that they disclose or make obvious the invention as claimed.

The Examiner has rejected claim 12 under 35 U.S.C. §103(a) as being unpatentable over U.S. Pat. No. 4,814,974 to Narayanan in view of U.S. Pat. No. 4,818,932 to Odenheimer and U.S. Pat. No. 5,581,722 to Welland and further in view of

U.S. Pat. No. 5,918,160 to Lysejko. Applicant has reviewed these references in detail and does not believe that they disclose or make obvious the invention as claimed.

Applicant notes with appreciation that the Examiner has indicated that claim 6 would be allowable if rewritten in independent form.

With regard to the double patenting rejection, the claims of the '715 patent are recited below:

> 1. A method for prioritizing access to a shared resource in a digital system having a plurality of devices vying for access to the shared resource, comprising the steps of:
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> initiating an access request by each of the plurality of devices;
>
> associating two priority values along with each access request from each device; and
>
> arbitrating for access to the shared device by using the higher of the two priority values associated with each single access request.
>
> 8. A digital system comprising:
>
> a shared resource;
>
> a plurality of devices connected to access the shared resource, wherein each device has an access priority register and a request output, wherein the access priority register of each device is loaded with a value by software executing on the respective device;
>
> a plurality of memory management units each connected to receive a virtual address from a respective one of the plurality of devices, wherein each memory management unit stores a plurality of page entries and has an output for an address space priority value contained in each page entry; and
>
> arbitration circuitry connected to receive a request signal from each request output along with an access priority value from each access priority register and an address space priority value from each memory management unit, wherein the arbitration circuitry is operable to schedule access to the shared resource according to the access priority value and the address space priority value.

The claims of '715 patent are directed to using multiple priority values to arbitrate multiple requests, which is significantly different than the present claims. Applicants will

consider the merits of filing a terminal disclaimer once allowable claims have been determined.

With regard to the §103(a) rejection of claim 1, it is important to note that Abe is directed to a cache controller and that the "priority" in Abe is not directed to prioritizing the order of servicing multiple pending requests to access the cache memory; rather, the "priority" in Abe determines whether an entry in the cache will be replaced with a currently accessed memory location. Whether an entry is replaced is determined on the priority of the currently accessed memory location. The priority for an entry is indicative of the frequency of access by the CPU 10 for accessing the data stored in the entry (col. 3, lines 61-64).

Hence, Abe does not prioritize access to a shared resource for multiple pending requests– it only determines whether a cache entry will be replaced or not.

Further, priority is assigned in Abe to individual memory addresses – not to an address space region including a plurality of addresses as set forth in amended claim 1. Further, it would be impossible to assign a priority to an address space region with multiple addressable locations, since in Abe, the priority is increased as each individual memory location is accessed.

Barnaby simply shows multiple devices accessing a shared resource, e.g. a DRAM. Combining Barnaby with Abe would simply lead to a device where the cache controller had entries for the most frequently accessed memory addresses. Abe does not prioritize *any type of multiple requests* based on *address space regions* – it only maintains cache entries based on the number of times an entry has previously been accessed.

Therefore, Applicants respectfully request allowance of claim 1 and dependent claims 2- 7.

Specifically, with regard to dependent claim 2, Abe makes no mention of assigning a priority value based on a program or data stored within a particular address space region. As noted above, this would be impossible, since Abe changes the priority of individual addresses each time they are accessed.

With regard to dependent claim 4, it would make no sense for Abe to assign a single access priority value to a single address space region occupied by a plurality of tasks, since Abe applies priority on individual addresses.

With regard to dependent claim 5, Abe does not show the steps of determining an access priority value specified by the program task, allocating an address space region for the program task and assigning the access priority value specified by the program task to the address space region allocated for the program task, since Abe teaches starting priority values at "0" and increasing the priority value for an address each time it is accessed (col. 5, lines 20-26).

With regard to claim 8, Narayanan teaches a *device-based* priority scheme where a priority for each device is assigned by a priority designator. When requesting access to a shared device, a REQUEST line (31-46) associated with the requesting system device is asserted. An arbitrator 27 selects one of the requesting devices through a GRANT line or lines (col. 4, lines 8-42). The arbitrator 27 selects among the requesting devices based on priority level uniquely associated with the devices.

Narayanan does not show a plurality of memory management units (MMU) each connected to receive an address from a respective one of the plurality of devices, wherein each MMU has storage circuitry *for storing a plurality of page entries and each page entry has an access priority value*, each MMU being operable to output the *access priority value associated with a received address*. Specifically, as discussed above, Narayanan does not have any teaching of access priority values based on page entries, or any other address region. Additionally, Narayanan does not show arbitration circuitry

connected to receive a request signal from each of the plurality of devices *and the associated access priority value* from each MMU, wherein the arbitration circuitry is operable to schedule access to the shared resource according to the access priority values.

Odenheimer does not teach prioritization for accessing a shared resource, where each *page entry* has an access priority value. Odenheimer specifically states the criteria for prioritization of multiple request signals: (1) a memory refresh is given the highest priority, (2) an access message to the digitizer is give the next highest priority, and (3) all other requests share the least highest priority. Once again, Odenheimer is clearly a device-based prioritization scheme, not a prioritization scheme based on the respective pages of memory being accessed (col. 9, lines 1-14).

Welland does not show page-based prioritization.

Accordingly, Applicants respectfully request allowance of claim 8 and dependent claims 9-12.

An extension of one month is requested and a Request for Extension of Time under § 1.136 with the appropriate fee is attached hereto.

The Commissioner is hereby authorized to charge any fees or credit any overpayment, including extension fees, to Deposit Account No. 20-0668 of Texas Instruments Incorporated.

Applicants have made a diligent effort to place the claims in condition for allowance. However, should there remain unresolved issues that require adverse action, it is respectfully requested that the Examiner telephone Alan W. Lintel, Applicants' Attorney at (972) 664-9595 so that such issues may be resolved as expeditiously as possible.

For these reasons, and in view of the above amendments, this application is now considered to be in condition for allowance and such action is earnestly solicited.

Respectfully Submitted,

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